7. A semiconductor device as recited in claim 6, wherein the plurality of supporting stubs are not electrically interconnected to the plurality of copper interconnect metallization lines and conductive vias.

8. A semiconductor device as recited in claim 6, further comprising:

a passivation layer defined over a topmost layer of the copper interconnect metallization lines and conductive vias.

21. (New) A semiconductor device, comprising:

a substrate having transistor devices; and

a plurality of copper interconnect metallization lines and conductive vias defined in each of a plurality of interconnect levels of the semiconductor device, the plurality of copper interconnect metallization lines and conductive vias being isolated from each other by a porous dielectric material.

REMARKS

The Examiner is thanked for his careful review of this Application. Claims 1-8 and 21 are pending after entry of the present Amendment. Please add new independent claim 21 and cancel non-elected claims 9-20. Amendments were made to the claims to clarify the claimed invention. These amendments do not introduce any new matter.

Objections to the Drawings under 37 CFR § 1.83:

Per the Office's request, the Applicants have added a new Figure 1F-3, showing the plurality of stubs, as defined in independent claim 6. As the stubs were included and defined in as-filed independent claim 6, it is submitted that the newly added Figure 1F-3 does not add any new matter. Accordingly, the Applicants respectfully request that the 37 CFR § 1.83(a) objections to the drawings be withdrawn.

Rejections under 35 U.S.C. § 102:

The Office has rejected claims 1-5 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,798,559 to Bothra et al. The Office has further rejected claims 1-5 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,078,088 to Buynoski. These rejections are respectfully traversed, as Bothra et al. fail to disclose each and every element of

the claimed invention, as defined in amended independent claim 1. Similarly, Buynoski fails to disclose each and every element of the claimed invention, as defined in amended independent claim 1.

Among other features, as amended, independent claim 1 defines that each of the plurality of supporting stubs is formed from the same contiguous material. Independent claim 1 further defines that each of the plurality of supporting stubs forms a filled supporting column that extends through the plurality of interconnect levels of the semiconductor device.

In contrast, Bothra et al. recite an integrated circuit structure that implements air as dielectric. The integrated circuit structure of Bothra et al. includes two level pillars, with the lower level being a dummy metallization layer and the upper level being a non-sacrificial oxide material that is supported by the dummy metallization layer. Bothra et al. also define one-level pillars made of non-sacrificial oxide material that are in direct contact with the metallization layers. The pillars of Bothra et al. are scattered in successive layers of the integrated circuit structure in any desired location so long as adequate support is provided.

Bothra et al. fail to disclose each and every feature of the claimed invention as defined in independent claim 1. Among other features, Bothra et al. disclose a plurality of two-tier pillars, with each tier being formed from a different material that are scattered within the layers of the integrated structure such that certain pillars are in contact with the metallization layers. In contrast, in the claimed invention, each of the plurality of stubs is formed from a contiguous material (i.e., one material and a single tier). Furthermore, each of the plurality of stubs forms a filled supporting column that extends through the plurality of interconnect levels of the semiconductor device. Two-tier pillars formed of different materials are not equivalent to the stubs of the claimed invention that are filled and are made of the same contiguous material.

Buynoski defines a liner to provide structural integrity. As taught, the liner should be formed from a material that is different than the metallization material. As further taught, the liner is applied so that metallization features are enveloped by the lining material. As defined above, the claimed invention defines a plurality of stubs that are formed from the same contiguous material and thus create filled supporting columns. A liner, as defined by Buynoski, simply cannot be equivalent to a filled supporting column.

Accordingly, independent claim 1 as amended, is respectfully submitted to be patentable under 35 U.S.C. § § 102(b) and 102(e) over Bothra et al. and Buynoski,

respectively. In a like manner, dependent claims 2-5 which directly or indirectly depend from independent claim 1 are submitted to be patentable over Bothra et al. and Buynoski for at least the same reasons set forth above regarding independent claim 1. As such, the Applicants respectfully request that the § § 102(b) and (e) rejections be withdrawn.

Rejections under 35 U.S.C. § 103:

The Office has rejected claims 6-8 under U.S.C. 103(a), as being unpatentable over Bothra et al. in view of U.S. Patent No. 6, 277,728 to Ahn et al. In a like manner, the Office has rejected claims 6-8 as being unpatentable under 35 U.S.C. 103(a) over Buynoski in view of Ahn et al. The Applicants respectfully traverse the Office's rejections and submit that independent claim 6, as amended, is patentable over the cited references, as none of the cited references would have suggested the claimed invention to one of ordinary skill in the art.

Independent claim 6 defines a semiconductor device that includes a substrate having transistor devices and a plurality of copper interconnect metallization lines and conductive vias defined in each of a plurality of interconnect levels of the semiconductor device. The plurality of copper interconnect metallization lines and conductive vias are isolated from each other by a porous dielectric material. The semiconductor device further includes a plurality of supporting stubs, each of which is configured to form a supporting column that extends through the plurality of interconnect levels of the semiconductor device.

Ahn et al., in contrast, define a multilevel interconnect structure that includes an outer low-k dielectric coating. The method of Ahn et al., in its broadest form, defines deposits a layer of photoresist on a substrate assembly followed by etching the photoresist to form openings. A metal layer is then deposited on the photoresist layer so as to fill the openings. Thereafter, the photoresist is removed and an upper level conductive metal layer is formed such that it is supported by the metal that filled the openings formed in the photoresist. Lastly, the upper level of the interconnect structure is then coated with a low-k dielectric film. Ahn et al. also teach planarizing the low-k dielectric coating.

Bothra et al. fail to motivate one having ordinary skill in the art to modify the integrated circuit structure that implements air dielectric and two-tier pillars scattered in the interlayers by using the low-k interlayer dielectric of Ahn et al. In column 2, lines 1-23, Bothra et al. enumerate several problems with implementing low dielectric constant materials instead of silicon dioxide and proceeds to dismiss and abandon the idea of using organic type dielectric materials in fabricating integrated circuits due to

being time consuming and requiring high fabrication costs. Thus, it is submitted that one having ordinary skill in the art, reading Bothra et al. and the teachings of Ahn et al., would not be motivated to implement low-k dielectrics instead of air.

Additionally, Bothra et al. simply disclose removing the sacrificial dielectric and do not replace the etched sacrificial dielectric. In fact, Bothra et al. achieve their goal of forming a low capacitance integrated device by leaving air as the dielectric. Ahn et al. follows Bothra et al.'s teachings of implementing interlayer air dielectric by just coating the outer surface of the multilevel interconnect structure with a low-k dielectric coating. In achieving the primary goal of reducing the number of dielectric deposition cycles, Ahn et al. use sacrificial photoresists having openings to create the interconnect metallization lines, contacts, and vias. Thus, the combination of Bothra et al. and Ahn et al. would not have encouraged one having ordinary skill in the art to add an extra deposition cycle for introducing a low-k dielectric, as defined in the claimed invention.

Additionally, Ahn et al. specifically define that the metallization lines are supported by the lower level metal layers. Thus, Ahn et al. do not suggest or motivate one having ordinary skill in the art to create any additional stubs to support the metallization lines or to use porous dielectric material to isolate the metallization lines and vias. Thus, the claimed invention, as defined in independent claim 6, is submitted to be patentable over Bothra et al. in view of Ahn et al.

It is further submitted that in contrast to the Office's assertion, the combination of liner of Buynoski and low-K coating of Ahn et al. would not have suggested the use of a plurality of stubs and the removal of sacrificial dielectric and replacement of same with porous dielectric. Especially due to Buynoski's statement that using of low-density materials having lower dielectric constant is costly and has a high degree of complexity and that using low-density materials results in a semiconductor device that lacks sufficient structural integrity. It must be noted that similar to Bothra et al., Buynoski abandons the idea of using low-K dielectric materials in favor of using air to reduce RC time delays.

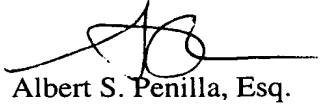
More importantly, Ahn et al. suggest planarizing the low-k dielectric coating. In doing so, Ahn et al. seems to ignore the challenges faced in planarizing the low-k dielectrics, disclosed by the Applicants. Thus, it is submitted that no combination of the cited prior art would have suggested the claimed invention and as such, the claimed invention is patentable over Buynoski in view of Ahn et al.

Therefore, it is respectfully submitted that dependent claims 7-8 which incorporate each and every element of independent claim 6 are patentable under 35 U.S.C. § 103(a) over Bothra et al. in view of Ahn et al. and Buynoski in view of Ahn et al. for at least the same reasons discussed above.

New independent claim 21, defines a semiconductor device that includes a substrate having transistor devices and a plurality of copper interconnect metallization lines and conductive vias defined in each of a plurality of interconnect levels of the semiconductor device. The plurality of copper interconnect metallization lines and conductive vias are isolated from each other by a porous dielectric material. It is submitted that new independent claim 21 is patentable over the cited art of record. None of the cited references teach using dielectric layers made of porous dielectric material. Additionally, each of the references discourage one of ordinary skill in the art to use the porous dielectric material to isolate the interconnect metallization lines, as discussed in more detail above.

In view of the foregoing, the Applicants respectfully submit that all of the pending claims are in condition for allowance. Accordingly, a Notice of Allowance is respectfully requested. If the Examiner has any questions concerning the present Amendment, the Examiner is kindly requested to contact the undersigned at (408) 749-6903. If any additional fees are due in connection with filing this Amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. LAM2P246). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
MARTINE & PENILLA, LLP



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Gotkis et al.

Application No: 09/821,415

Filed: March 28, 2001

For: SEMICONDUCTOR STRUCTURE IMPLEMENTING LOW-K DIELECTRIC MATERIALS AND SUPPORTING STUBS (As Amended)

Atty. Docket: LAM2P246

Examiner: H.K. Vu

Group Art Unit: 2811

Date: July 24, 2002

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231 on July 24, 2002.

Signed: _____
Courtney F. Yadegar

MARKED-UP TITLE AND CLAIMS

IN THE TITLE

Please amend the Title to state:

"Semiconductor Structure Implementing **[Sacrificial Material and Methods for Making and Implementing the Same]** **Low-K Dielectric Materials and Supporting Stubs**"

IN THE CLAIMS

1. **(Amended)** A semiconductor device, comprising:

a substrate having transistor devices;

a plurality of copper interconnect metallization lines and conductive vias defined in each of a plurality of interconnect levels of the semiconductor device, the plurality of copper interconnect metallization lines and conductive vias isolated from each other by an air dielectric; and

a plurality of supporting stubs, each of the plurality of supporting stubs configured to **be formed from a same contiguous material, each of the plurality of supporting stubs further configured to** form a **filled** supporting column that extends through the plurality of interconnect levels of the semiconductor device.

21. (New) **A semiconductor device, comprising:**

a substrate having transistor devices; and

a plurality of copper interconnect metallization lines and conductive vias defined in each of a plurality of interconnect levels of the semiconductor device, the plurality of copper interconnect metallization lines and conductive vias being isolated from each other by a porous dielectric material.

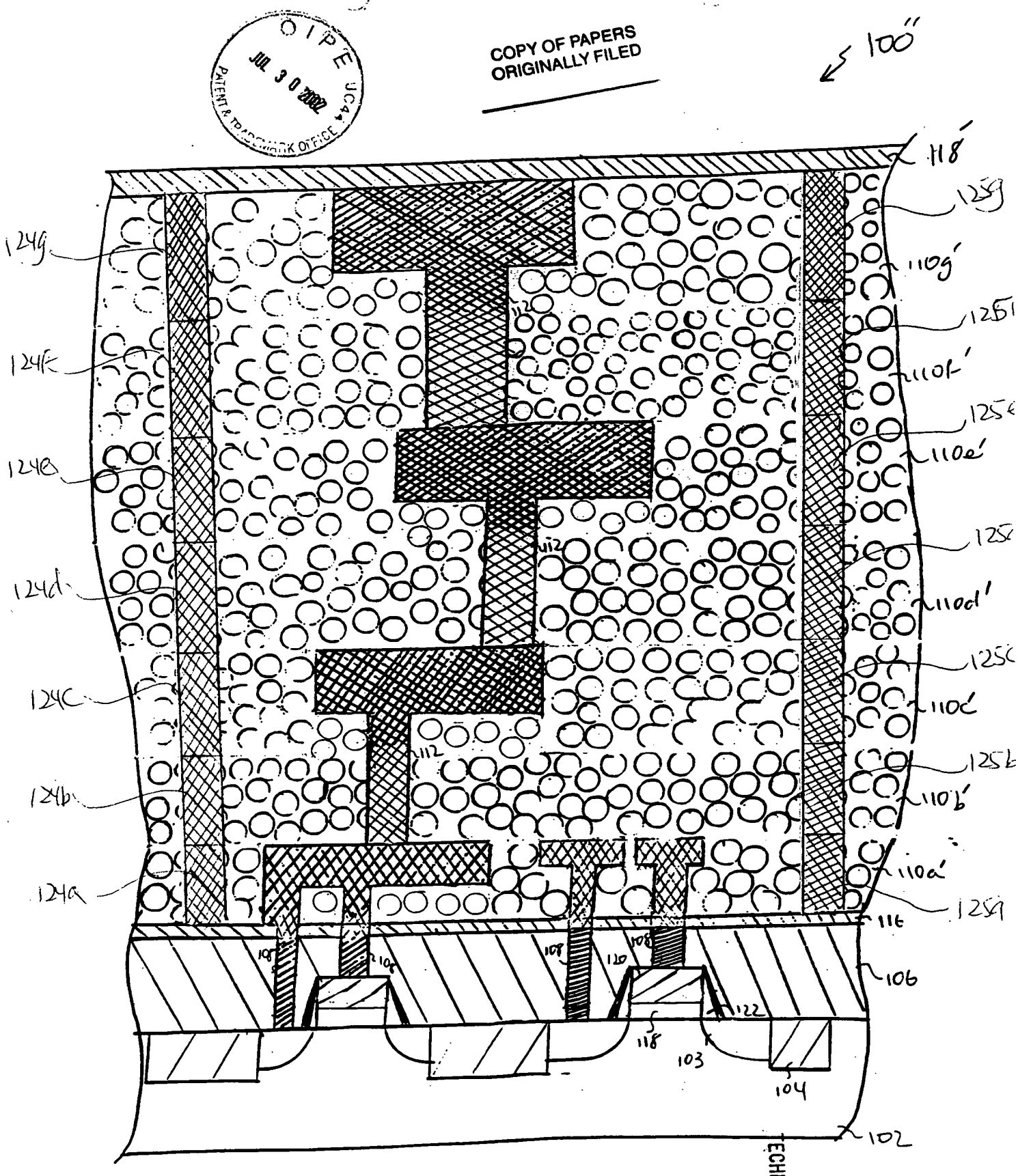

FIG 1F-3